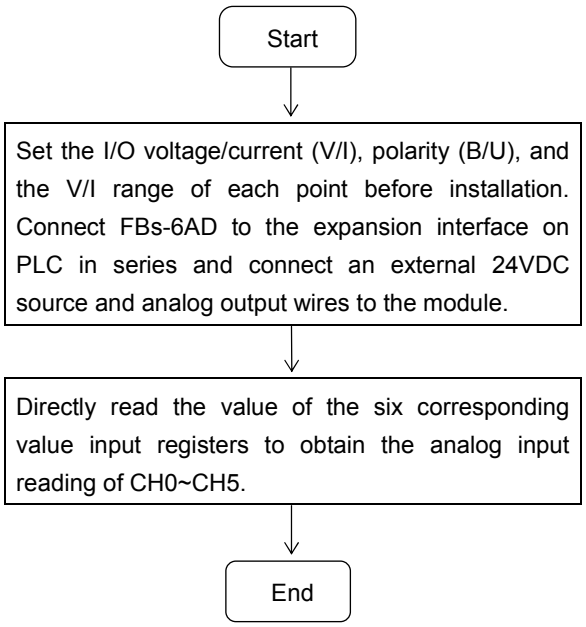
Chapter 18 FBs-6AD Analog Input Module

FBs-6AD is one of the analog input modules of FATEK FBs series PLC. It provides 6 channels A/D input with 12 or 14 bits effective resolution.. Base on the different jumper settings it can measure the varieties of current or voltage signal. The reading value is represented by a 14-bit value no matter the effective resolution is set to 12 or 14 bits. In order to filter out the field noise imposed on the signal, it also provides the average of sample input function.

18.1 Specifications of FBs-6AD

Item			Specifications	Remark
Total Channel			6 Channel	
Digital Input Value			–8192～+8191or 0～16383(14 bits) –2048～+2047or 0～4095(12 bits)	
Span Of Analog input	Bipolar*	10V*	*1.Voltage：–10～10V 5.Current：–20～20mA	* ： It means the default setting
		5V	2. Voltage：–5～5V 6. Current：–10～10mA	
	Unipolar	10V	3. Voltage：0～10V 7. Current：0～20mA	
		5V	4. Voltage：0～5V 8. Current：0～10mA	
Resolution			14 or 12 bits	
Finest resolution			Voltage：0.3mV Current：0.61μA	= Analog input signal / 16383
I/O Points Occupied			6 IR(Input Register)	
Accuracy			Within ±1% of full scale	
Conversion Time			Updated each scan	
Maximum absolute input signal			Voltage：±15V（max） Current：±30mA（max）	It may cause the destruction to hardware if exceeds this value.
Input resistance			63.2KΩ（Voltage input）、250Ω（Current input）	
Isolation			Transformer(Power) and photocouple(Signal)	
Indicator(s)			5V PWR LED	
Supply Power			24V-15%/+20%、2VA	
Internal Power Consumption			5V、100mA	
Operating Temperature			0 ~ 60 ℃	
Storage Temperature			-20 ~ 80 ℃	
Dimensions			40(W)x90(H)x80(D) mm	

18.2 The procedure of Using FBs-6AD module



------- Please refer to section 18.4 for hardware explanation.

18.3 Address allocation of FBs-PLC analog inputs

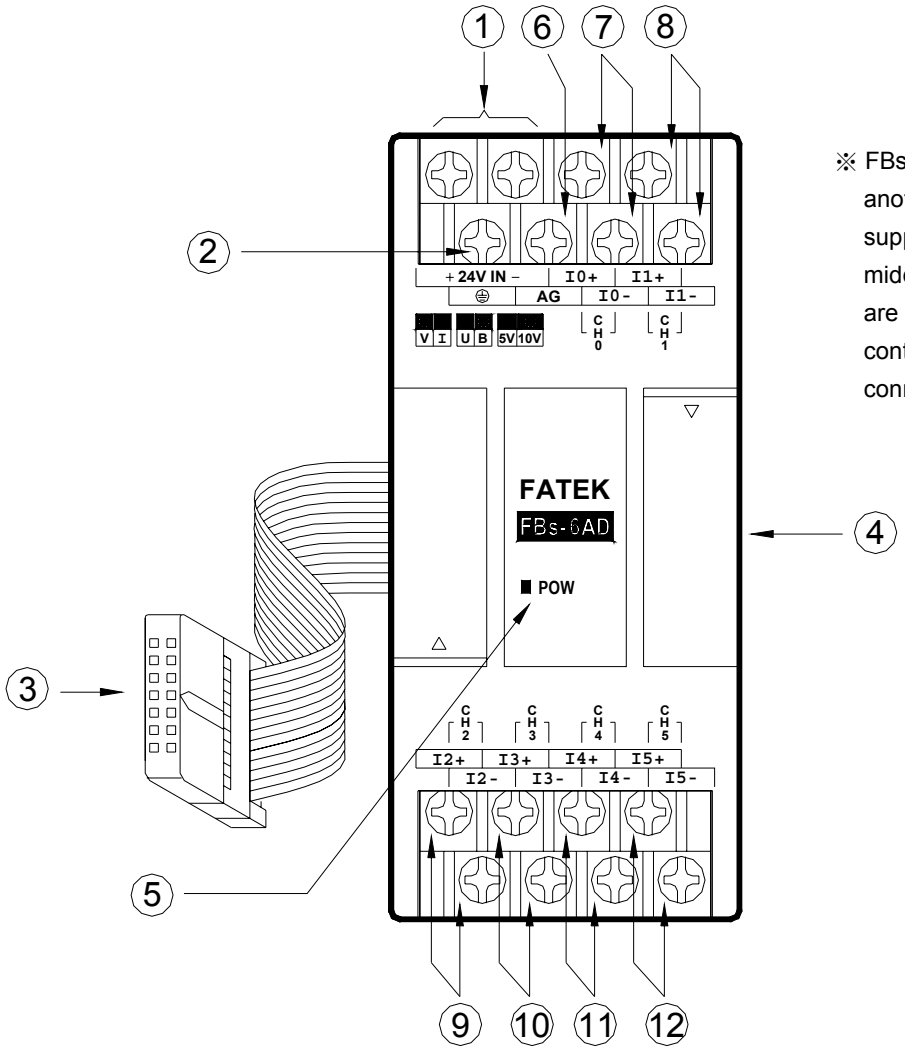
The I/O addressing of FBs-6AD inputs is beginning from the module closest to main unit, it is orderly numbered as CH0～CH5 (1st module), CH6～CH11 (2nd module), CH12～CH17 (3rd module)…… and increased with occurring order number, i.e. for each module, it adds with 6 and is totally 64 inputs from CH0～CH63, and they are corresponding to the respective internal analogue input register of PLC (so called as IR register) R3840～R3903 as listed in following table. After connecting FBs-6AD to the expansion interface on the PLC, FBs-PLC will automatically detect the number of AD points. WinProladder will automatically detect and calculate the IRs on the system after connecting to the PLC. Users may refer to the I/O Module Number Configuration provided by WinProladder in order to find out the exact I/O address of each expansion module to facilitate programming.

Numeric Input Register（IR）	Content of IR (CH0～CH63)	Input lable Of FBs-6AD	
	B_{15} B_{14} B_{13} B_{12} B_{11} B_{10} B_9 B_8 B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0		
IR+0	14/12 bit ; 14-bit , B14~ B15= B13 ; 12-bit, B12~ B15= B11	CH0	FBs-6AD
IR +1	14/12 bit ; 14-bit , B14~ B15= B13 ; 12-bit, B12~ B15= B11	CH1	
IR +2	〃	CH2	
IR +3	〃	CH3	
IR +4	〃	CH4	
IR +5	〃	CH5	
IR +6	Depends on module type	CHX	
IR +7	Depends on module type	CHX	
IR +8	〃	CHX	
IR +9	〃	CHX	

≈	≈	≈
R3896	〃	CHX
R3897	〃	CHX
R3898	〃	CHX
R3899	〃	CHX
R3900	〃	CHX
R3901	〃	CHX
R3902	Depends on module type	CHX
R3903	Depends on module type	CHX

Other Modules

18.4 FBs-6AD hardware description



※ FBs-6AD contains 3 PCBs overlapping one another. The lowest one is the power supply unit (isolated power supply). The middle one is the I/O board (connectors are on this layer). The upper one is the control board (control/expansion I/O connections) as described below.:

Outlook of top view

① External power input terminal ：Power supply of analogue circuit for FBs-6AD, the voltage can be 24VDC±20% and should be supplied with 4W of power at least.

② Protecting ground terminal：Connect to the shielding of the signal cable.

③ Expansion input cable：It should be connected to the front expansion unit, or the expansion output of main unit.

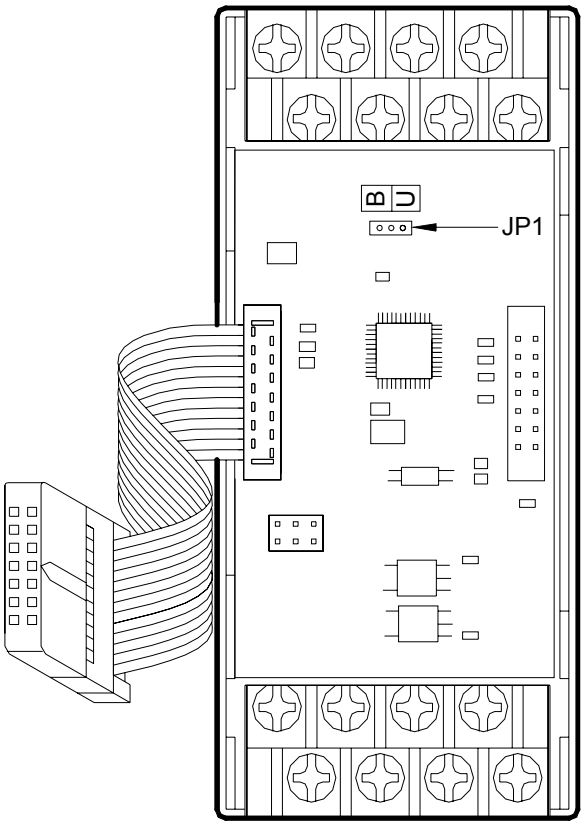
④ Expansion output connector：Provides the connection for next expansion unit.

⑤ Power indicator： It indicates whether the power supply at analogue circuit and external input power source are normal.

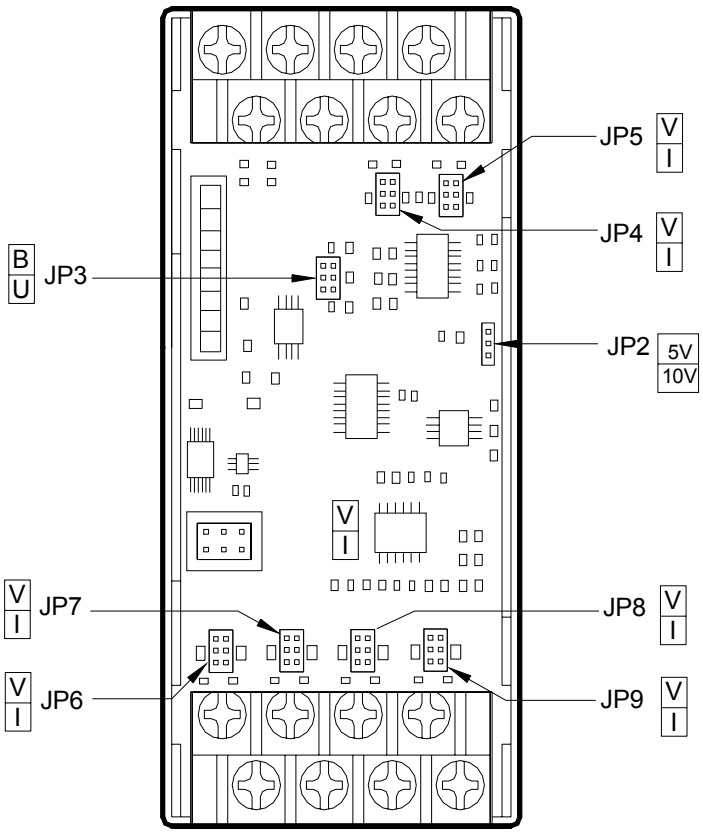
⑥ AG Ground：No connection is needed in general; except when the common mode signal is too high. See examples overleaf for details.

⑦～⑫：Input terminal of CH0～CH5.

18.4.1 FBs-6AD hardware jumper setting



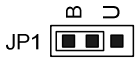
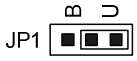
Pin layout in control board (open top cover)



Pin layout on I/O board (remove control board)

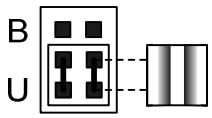
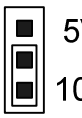
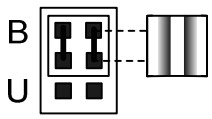
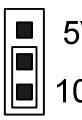
1. Input code format selection (JP1)

Users can select between unipolar and bipolar codes. The input range of unipolar codes and bipolar codes is 0~16383 and –8192~8191, respectively. The two extreme values of these formats correspond to the lowest and highest input signal values, respectively (see table below). For example, if the input signal type is set to -10V~ +10V, the unipolar code corresponding to the input is 8192 and the bipolar code corresponding to the input is 0 for 0V input. If the input is 10V, the unipolar code corresponding to the input is 16383 and the bipolar code corresponding to the input is 8191. In general, the input code format is selected according to the form of input signals; i.e. unipolar codes for unipolar input signals; and bipolar codes for bipolar input signals. In doing so, their correlations will become more heuristics. Unless it is necessary to make a deviation conversion through FUN32; otherwise, do not select bipolar codes for unipolar input signals (see FUN32 description for details). The format of input codes of all channels is selected from JP1. See above diagram for the location of JP1：

Input Code Format	JP1 Setting	Input Value Range	Corresponding Input Signals
Bipolar		-8192～8191	-10V～10V(-20mA～20mA) -5V～5V(-20mA～20mA)
Unipolar		0～16383	0V～10V(0mA～20mA) 0V～5V(0mA～10mA)

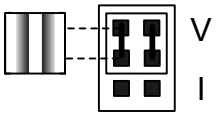
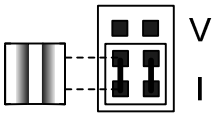
2. Input signal form setup (JP2&JP3)

Users can set the input signal form (voltage/current) of individual channels; except the polarity and amplitude which are common. The location of jumpers are tabulated below：

Signal Form	JP3 Setting	JP2 Setting
0～10V or 0～20mA		
0～5V or 0～10mA		
-10～+10V or -20～+20mA		
-5～+5V or -10mA～+10mA		

CH0~CH5 share the JP2 and JP3 jumper, therefore all channels must be of the same type that is one of the four types listed at above table. Only the current/voltage setting can be chosen arbitrary：

3. Voltage or current setting (JP4～JP9)

Signal Type	JP4(CH0) ～ JP9(CH5) Setting
Voltage	
Current	

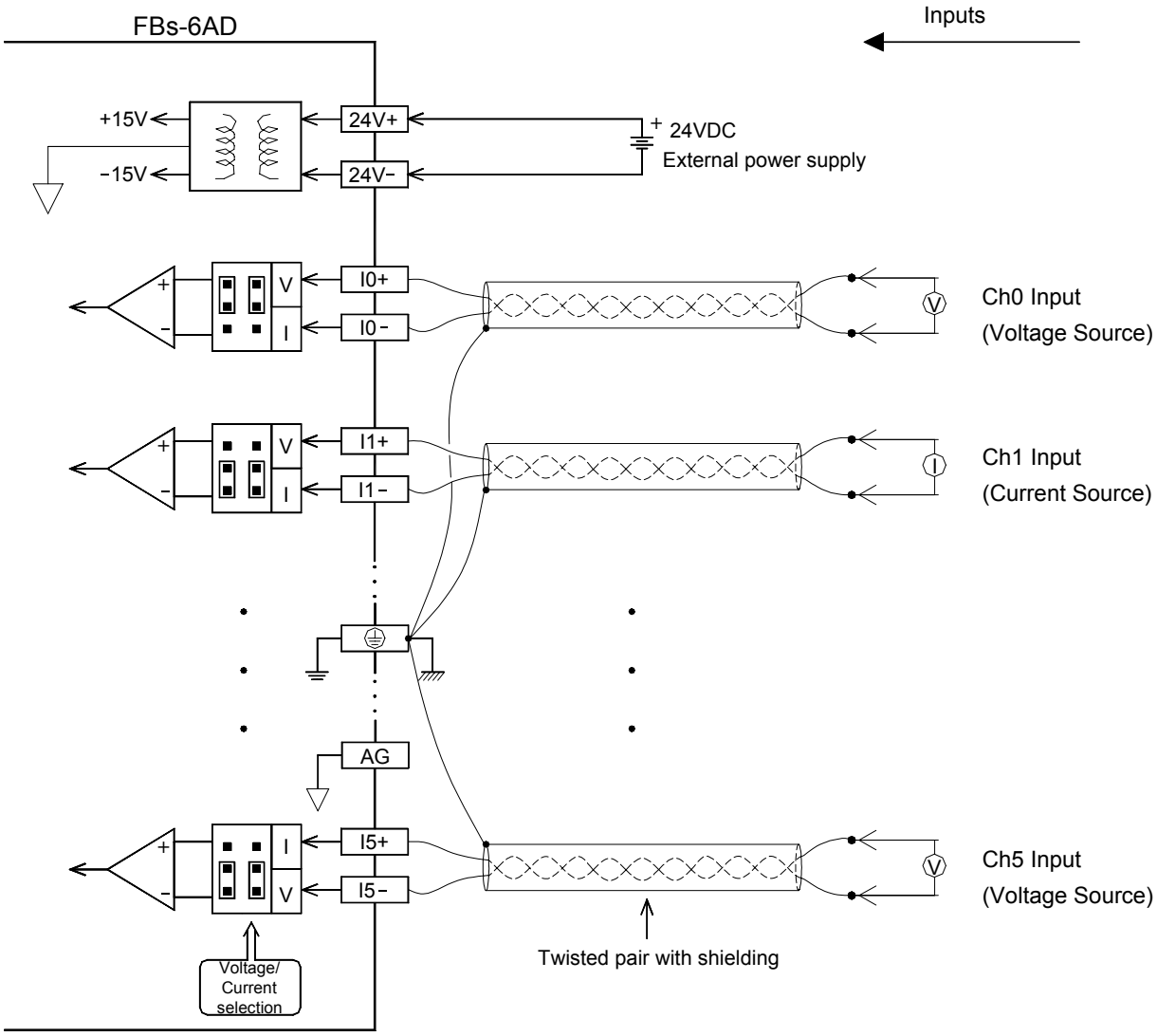
＊The default factory settings of 6AD analogue input module are：

Input code format → Bipolar(-8192~+8191)

Input signal type and range → Bipolar(-10V ~ +10V)

For those applications that require the setting differ than the above default setting should make some modifications of jumper position according to above tables. While application, besides the setting of jumper should be conducted, the AI module configuration of Winproladder also need to be performed.

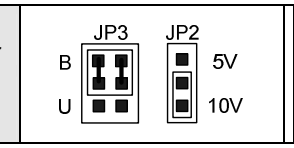
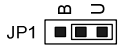
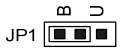
18.5 FBs-6AD input circuit diagram



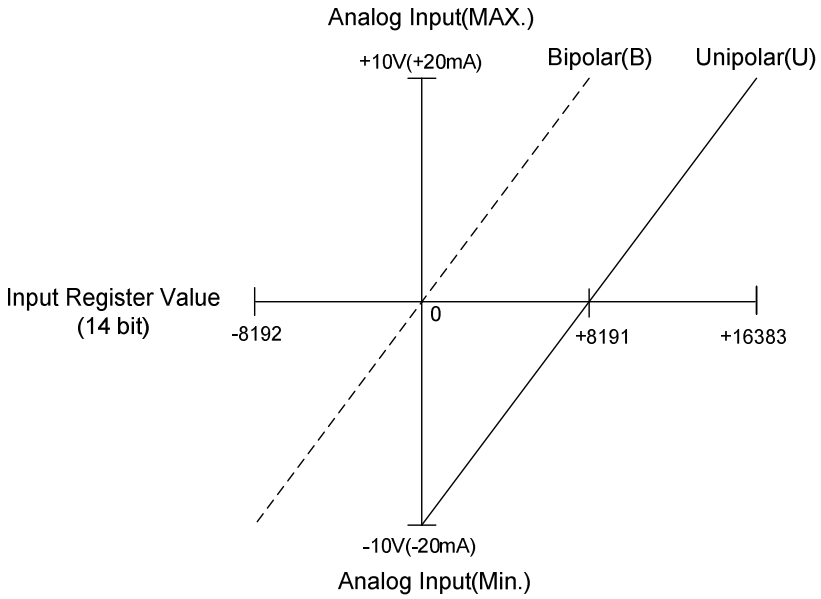
18.6 FBs-6AD input characteristics and jumper setting

Users can select the Input ranges of FBs-6AD from the jumpers described above, such as V/I, U/B (I/O codes), U/B (signal form), 5V/10V, etc. The Input signals conversion characteristics of these settings are illustrated below. Users can adjust different Input forms by coordinating the conversion curve with various V/I (voltage/current) Input settings. See Section 18.4 for details of V/I settings **:**

Diagram 1：Bipolar 10V（20mA）Span

Input Range	Voltage	−10V～10V	Jumper Setting		———— 
	Current	−20mA～20mA			- - - - - - - - 

14 bit input format



12 bit input format

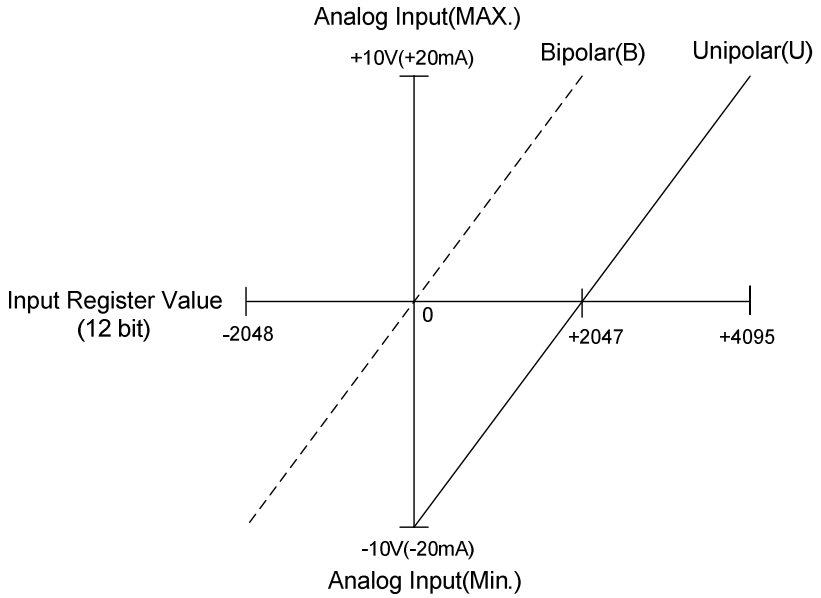
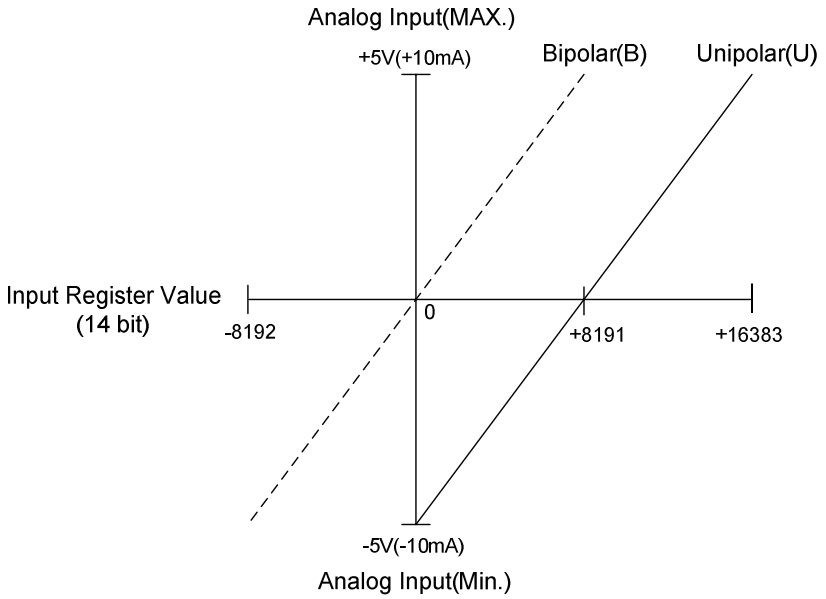


Diagram 2：Bipolar 5V（10mA）Span

Input Range	Voltage	−5V～5V	Jumper Setting	JP3 JP2 B 5V U 10V	———— JP1 B U
	Current	−10mA～10mA			- - - - - - - - JP1 B U

14 bit input format



12 bit input format

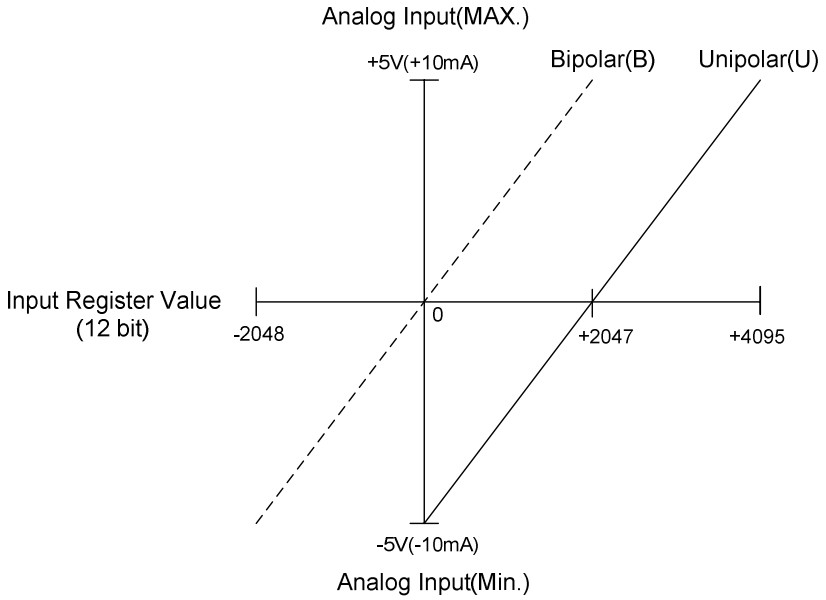
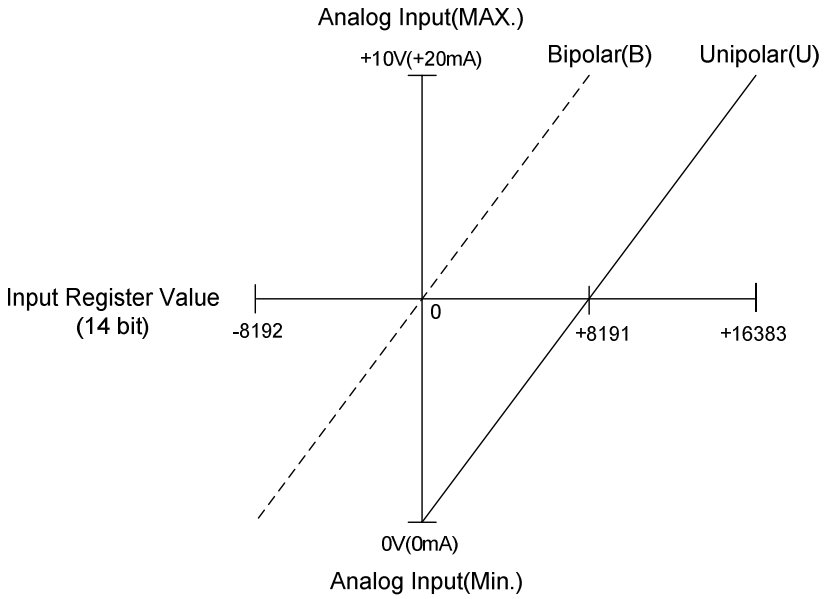


Diagram 3：Unipolar 10V（20mA）Span

Input Range	Voltage	0V～10V	Jumper Setting	JP3 JP2 B 5V U 10V	———— JP1 B U
	Current	0mA～20mA			-------- JP1 B U

14 bit input format



12 bit input format

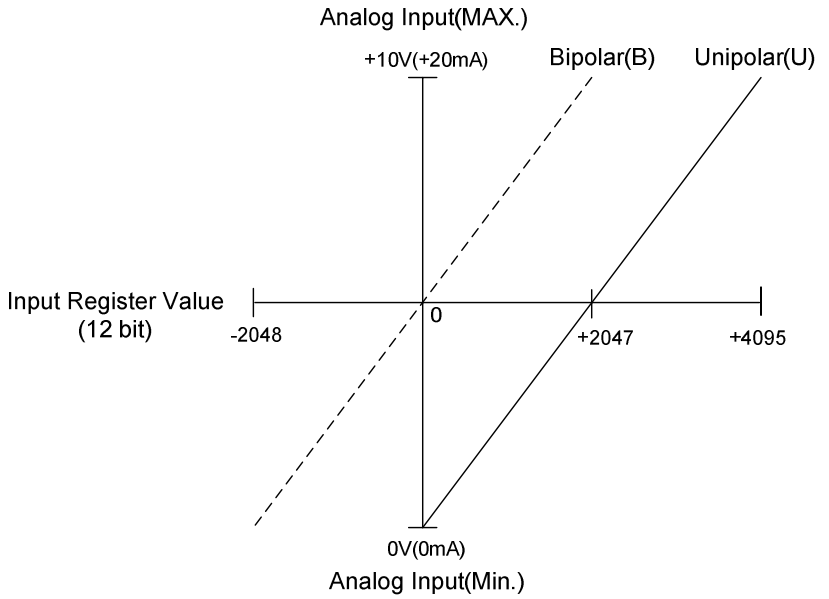
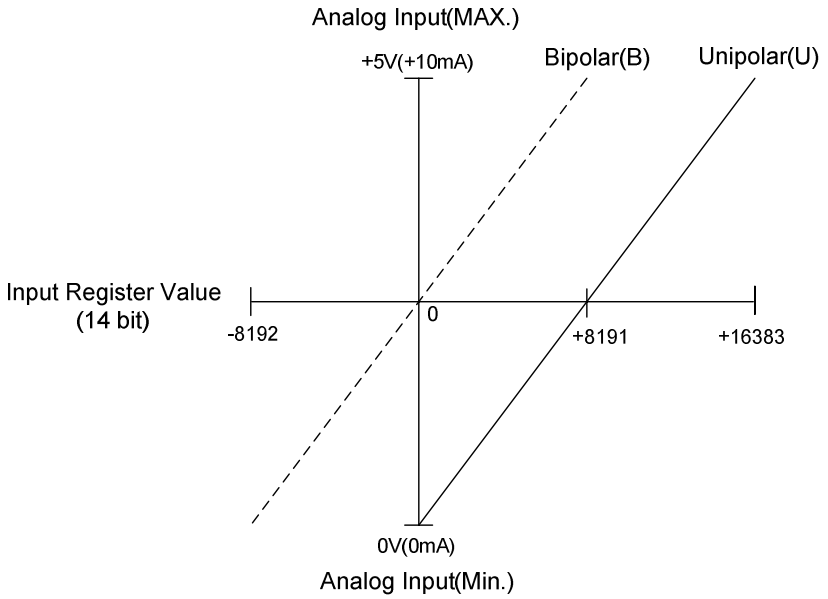


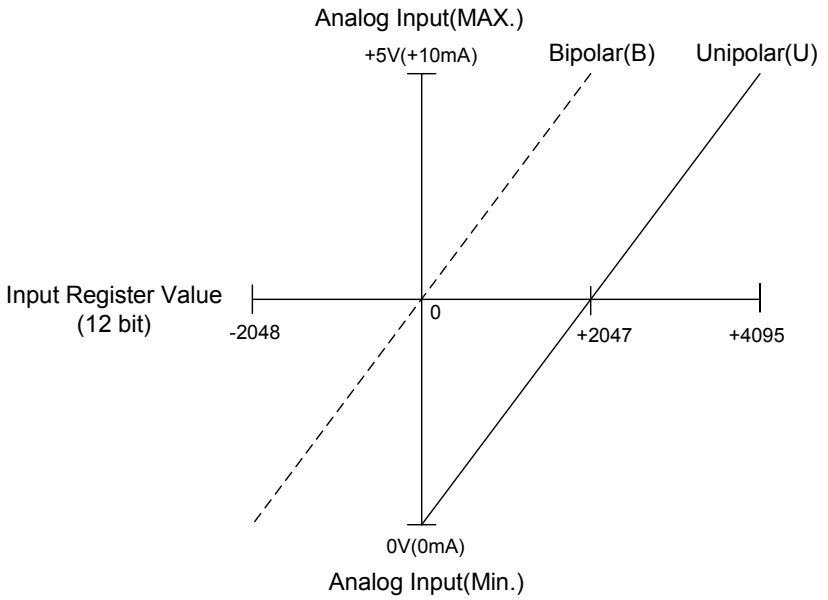
Diagram 4：Unipolar 5V（10mA）Span

Input Range	Voltage	0V～5V	Jumper Setting	JP3 JP2 B 5V U 10V	————	JP1 B U
	Current	0mA～10mA			- - - - - - - -	JP1 B U

14 bit input format



12 bit input format



18.7 Configuration of analog input

For the analog input reading of FBs series PLC, there are 3 kinds of data formats used to represent the reading value in compliance with the variation of the external analog inputs. Also, it supports the average method to improve the drift of the reading value away from the noise interference or unstable original analog signal.

The WinProladder provides the friendly and convenient operation interface for the purpose of analog input configuration. There are "analog input data format", "valid bits", and "number of average" for settings.

The procedures for analog inputs configuration with WinProladder

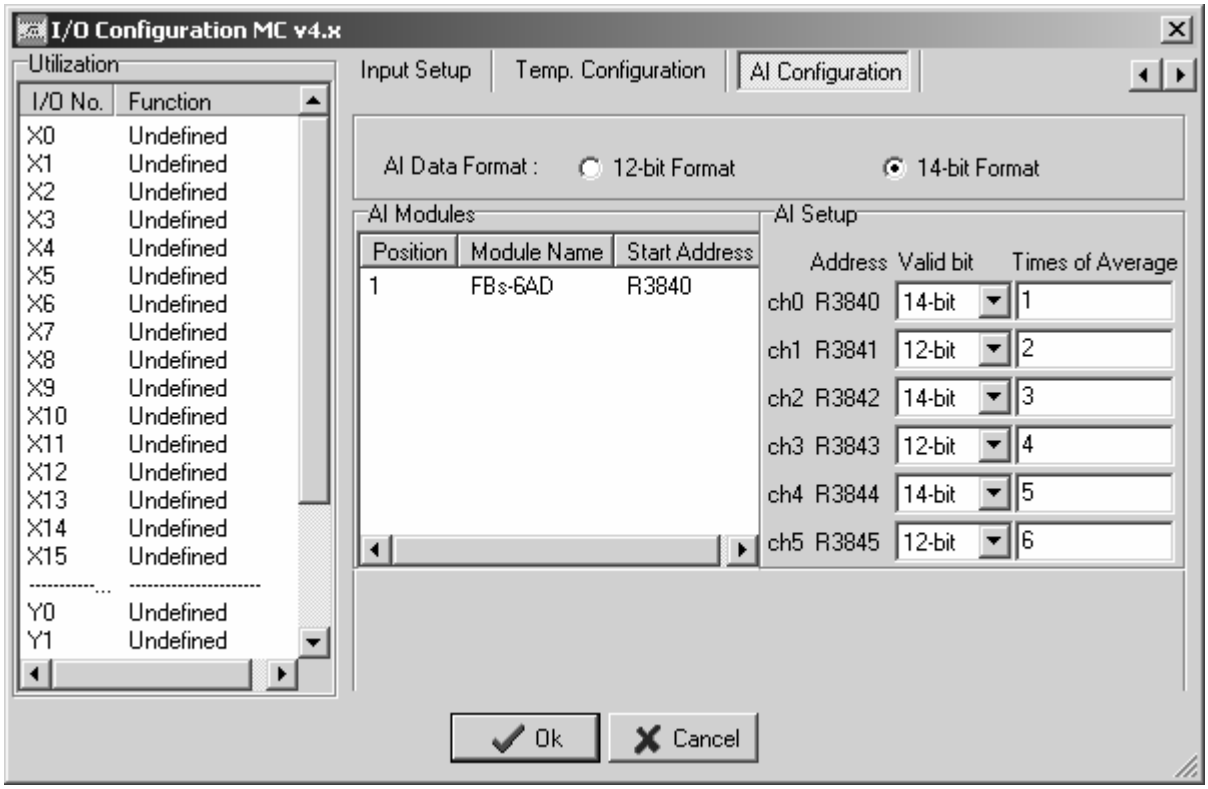
Click the item “I/O Configuration” which in Project Windows **:**

Project name

System Configuration

I/O Configuration → Select “AI Configuration”

- If FBs main unit connects with AD Expansion nodule, then it will auto detect and allotted the system resource(IR).



Description of the configuration screen：

- AI Data Format ：All analog inputs can be assigned as 12-bit or 14-bit resolution of data format.

- AI Modules ：This window displays the information of installed analog input modules, click the selective module will bring the setting window for valid bits and times of average.

- AI Setup ：When the data format is 12-bit resolution, each channel of analog input can be allowed to set the times of average; When the data format is 14-bit resolution, each channel of analog input can be allowed to set the valid bits and times of average.

AI Data Format

● 12-bit resolution with sign representation (-2048～2047)：

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
B11	B11	B11	B11	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

＊B11 = 0--------- Positive reading value
1--------- Negative reading value
＊B15～B12 = B11

● 12-bit resolution without sign representation (0～4095)：

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

● 14-bit but valid 12-bit resolution with sign representation (-8192～8188)：

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
B13	B13	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0

＊B13 = 0--------- Positive reading value
1--------- Negative reading value
＊B15～B14= B13 ; B1～B0= 0

＊In this Data Format, because B1 and B0 are fixed 0 then value change by times of 4.

● 14-bit but valid 12-bit resolution without sign representation (0～16380)：

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0

＊In this Data Format, because B1 and B0 are fixed 0 then value change by time of 4.

● 14-bit resolution with sign representation (-8192～8191)：

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
B13	B13	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

＊B13 = 0--------- Positive reading value
1--------- Negative reading value
＊B15～B14= B13 ; B1～B0= 0

● 14-bit resolution without sign representation (0～16383)：

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Relative registers of AI configuration

This introduction is for HMI or SCADA User, because they may modify through registers. Winprolader's User can ignore this introduction. When you configure Analog Input format with Winproladder, these value of registers will be finished.

Register	Content	Description
D4042	5612H	all analog inputs are the 12-bit resolution ; it is allowed to set times of average for each channel.
〃	5614H	all analog inputs are the 14-bit resolution ; it is allowed to set times of average for each channel.

Register	Content	Description
D4006	B0 = 0	AI channel 0 is valid 12-bit resolution.
	B0 = 1	AI channel 0 is valid 14-bit resolution.
〃	⋮	⋮
D4006	B15 = 0	AI channel 15 is valid 12-bit resolution.
	B15 = 1	AI channel 15 is valid 14-bit resolution.
D4007	B0 = 0	AI channel 16 is valid 12-bit resolution.
	B0 = 1	AI channel 16 is valid 14-bit resolution.
〃	⋮	⋮
D4007	B15 = 0	AI channel 31 is valid 12-bit resolution.
	B15 = 1	AI channel 31 is valid 14-bit resolution.

Register	Content	Description
D4008	B0 = 0	AI channel 32 is valid 12-bit resolution.
	B0 = 1	AI channel 32 is valid 14-bit resolution.
〃	⋮	⋮
D4008	B15 = 0	AI channel 47 is valid 12-bit resolution.
	B15 = 1	AI channel 47 is valid 14-bit resolution.
D4009	B0 = 0	AI channel 48 is valid 12-bit resolution.
	B0 = 1	AI channel 48 is valid 14-bit resolution.
〃	⋮	⋮
D4009	B15 = 0	AI channel 63 is valid 12-bit resolution.
	B15 = 1	AI channel 63 is valid 14-bit resolution.

Register	Content	Description
D4010	1～16	Low byte is used to define the times of average for AI channel 0.
	1～16	High byte is used to define the times of average for AI channel 1.
⋮	⋮	⋮
D4041	1～16	Low byte is used to define the times of average for AI channel 62.
	1～16	High byte is used to define the times of average for AI channel 63.

※ The default of AI data format is 14-bit resolution, valid 12-bit, and times of average is 1.

※ The legal setting value for times of average is 1～16, if it is not the value：

The default for times of average is 1 when it is valid 12-bit resolution.
The default for times of average is 8 when it is valid 14-bit resolution.

18.8 Tackling on the OFFSET mode input

For the process of input for signal source of offset mode (take 4～20mA input for example), the user can set A/D input range to be 0～20mA, convert the IR value to unipolar (0～16383), lessen the offset (4mA) value (16383x4/20=3276), then times the maximum input amount (20mA), and divide by the maximum span (4mA～20mA); and it can acquire the offset input conversion from 4mA～20mA reflect to 0～16383, the procedure is as follows：

a. Set the A/D input range of analogue input module to be 0～20mA.

b. Add the IR (R3840～R3903) value with * 8192 and then store it into register Rn (the value of Rn is 0～16383).

c. Deduct 3276 ($16383 \times \frac{4}{20}$) from value of register Rn, and store the calculated value back to register Rn; if the value is negative, clear the content of register Rn to 0 (the value of Rn is 0～13107).

d. The value of register Rn times 20 and then divide by 16 (Rn x $\frac{20}{16}$), and it will convert the 4mA～20mA input to range of 0～16383.

e. To sum up the items from a～d, the mathematical equation is as follows：

Offset mode conversion value = 〔 IR+8192(or 0) – (16383× $\frac{4}{20}$)〕× $\frac{20}{16}$ ； value is 0～16383

※ Special to 4～20 mA Offset mode, you can use FUN32 to substitute for processing above, but another offset mode please refer to above processing.

* note : Step b “Add 8192” is means input code setting in bipolar mode(JP1 setting in position B). If input code setting in unipolar mode (JP1 setting in position U) then you don’t have to “Add 8192”.